Examiner's argument that single chip 200 includes a processor is without support from Beaudoin.

First, Figure 1 includes a block diagram of multiport, multipurpose network integrated circuit (chip) 200. No processor or CPU is shown. Second, Beaudoin very specifically states that it is an object of the invention not to utilize a processor or CPU when implementing the functionality of multiport, multipurpose network integrated circuit (chip) 200. Specifically, Beaudoin states the following: "It is an object of the present invention to provide apparatus and methods for hardware control of network switching functions rather than CPU based control." See column 2, lines 55 through 57. Thus, Examiner's argument that multiport, multipurpose network integrated circuit (chip) 200 contains a processor/CPU appears to be directly contradicted by the subject matter disclosed by Beaudoin. In any event, it is very clear that Beaudoin does not disclose or suggest a processor within multiport, multipurpose network integrated circuit (chip) 200.

Response to Second Argument

Examiner has argued as follows:

> Further, Beaudoin states that control, logic and communications are performed by the processes in the single chip, which is not unlike the embedded processor claimed in the instant application.

See the Office Action dated July 1, 2003 at page 5, lines 2 through 4.

Actually, the functionality of the embedded processor set out in claim 1 of the present application is very much "unlike" the control, logic and

communications performed by the entities in the single chip multiport, multipurpose network integrated circuit (chip) 200.

Specifically, Claim 1 sets out functionality of the embedded processor. The embedded processor is programmable to function as a manageability web server, communicates with the host interface and obtains manageability information about the network device.

This functionality is clearly not performed by any entity within single chip multiport, multipurpose network integrated circuit (chip) 200. No entity within single chip multiport is programmable to function as a manageability web server. No entity within single chip multiport, multipurpose network integrated circuit (chip) 200 communicates with a host interface. No entity within single chip multiport, multipurpose network integrated circuit (chip) 200 obtains manageability information about the network device.

Further, Examiner appears to be asserting an improper standard to determine whether a reference anticipates an element of a claim. The standard is not whether, in a vague way, functionality in a reference is "not unlike" an element of a claim. Rather, as further discussed below, the standard is as follows: "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Response to Third Argument

Examiner has argued as follows:

> The manageability web server, as claimed, communicates with the host interface, the processor of Beaudoin shows this in the figure 1 by way of the bi-directional arrows pointing inside single chip 200 and outside single ship 200.

See the Office Action dated July 1, 2003 at page 5, lines 7 through 10.

In this statement, Examiner assumes the existence of two entities that are clearly not shown in Figure 1 of Beaudoin.

First Examiner assumes the existence of a "host interface". However, the existence of "host interface" would seem to indicate the existence of a host, i.e., an external (host) processor.

However, Examiner's entire argument for the existence of an "embedded processor" within single chip multiport, multipurpose network integrated circuit (chip) 200 is based on Examiner's assertion that the "absence of an external processor indicates that Beaudoin discloses a processor on single chip 200". So Examiner has asserted there is no external (host) processor, but there must be a host interface????

Why is there a host interface when there is no host processor?

Clearly, Figure 1 of Beaudoin does not disclose a host interface. If Figure 1 of Beaudoin did disclose a host interface, the existence of the host interface would demolish Examiner's sole rationale for the existence of an "embedded processor" within single chip multiport, multipurpose network integrated circuit (chip) 200.

Second, Examiner assumes the existence of a manageability web server within single chip multiport, multipurpose network integrated circuit (chip)

200. However, it is impossible to determine what entity within single chip multiport, multipurpose network integrated circuit (chip) 200 Examiner regards as functioning as a manageability web server.

The only clue Examiner has given is that manageability web server is connected to a bi-directional arrow. However, in Figure 1, none of the entities connected to a bi-directional arrow (MAC 120, 122, 124, FIFOs 130, queue manager 140, LED interface 182, EEPROM interface 80, DRAM controller 142, statistics RAM 168, DIO interface 170) function as a manageability web server.

**Specific Discussion of Claim Rejections**

Examiner has rejected claims 1 through 3, 5 through 15 and 21 through 30 under 35 U.S.C. § 102(e) as being anticipated by USPN 6,400,715 (Beaudoin). Examiner has rejected claims 4 and 16 through 18 under 35 U.S.C. § 103(a) as being unpatentable over Beaudoin in view of USPN 5,903,737 (Han). Examiner has rejected claims 19 and 20 under 35 U.S.C. § 103(a) as being unpatentable over Beaudoin. Applicant respectfully traverses the rejections and requests reconsideration.

**Criteria for a Rejection under 35 U.S.C. § 102**

The criteria for a rejection under 35 U.S.C. § 102 has been clearly defined by the courts and confirmed by the U.S. Patent and Trademark Office. "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art

reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

**Criteria for a Rejection under 35 U.S.C. § 103(a)**

The U.S. Patent and Trademark Office has set forth a methodology for establishing a *prima facie* case of obviousness. Specifically, three basic criteria must be met.

> First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations.

See MPEP 706.02 (j).

**Overview of Reason for Traversal**

All the independent claims were rejected under 35 U.S.C. § 102 (e). However, Examiner has failed to show that each and every element set forth in the independent claims is found either expressly or inherently in Beaudoin.

Below, Applicant clearly and unambiguously points out subject matter within each independent claim that is not disclosed or suggested by Beaudoin. On the basis of this, Applicant believes all the claims are patentable over Beaudoin, whether considered alone or in combination with Hans.

## Brief Description of Beaudoin

Beaudoin discloses a network address matching circuit and method. A circuit 200, preferably implemented on a single chip, consists of Ethernet media access control (MAC) blocks 1201,1221,1241, a first-in first-out (FIFO) RAM block 1301, a DRAM interface block 1421, a queue manager block 1401, an address compare block 150, an EEPROM interface block 801, a network monitoring multiplexer (mux) block 1601, an LED interface block 1801, a DIO interface block 1701, an external address interface block 184 and network statistics block 1681. Each of the MACS 1201, 1221, 1241 is associated with a communications port 116,117,118 of the circuit 200; thus, the circuit 200 has fifteen available communications ports for use in a communications system of the present invention. See column 14, lines 47 through 65.

## Brief Description of Han

Han discloses an apparatus and method for serial data communication utilizing general microcomputer.

## Discussion of Independent Claim 1

Independent claim 1 sets out a chip for incorporation within a network device connectable to a computer network. The chip includes a media access controller, a host interface and an embedded processor.

Embedded Processor

The embedded processor is between the host interface and the media access controller. The embedded processor is programmable to function as a manageability web server, communicate with the host interface and obtain manageability information about the network device. The embedded processor further is programmable to send the manageability information to the media access controller for transmission over the computer network. None of this functionality is disclosed or suggested by Beaudoin, whether considered alone or in combination with Han.

The Examiner has asserted that multiport, multipurpose network integrated circuit (chip) 200 of Beaudoin includes an embedded processor. Examiner appears to be making this assertion based on the statement by Beaudoin at column 15, lines 5 through 7: "More particularly, this consolidation results in the elimination of the need for an external CPU to control, or coordinate control, of all these functions."

However, this statement in Beaudoin does not specifically state that multiport, multipurpose network integrated circuit (chip) 200 includes an embedded processor, but only indicates that there is no need for an external CPU to control or coordinate control of functions performed by multiport, multipurpose network integrated circuit (chip) 200.

As discussed above, Figure 1 includes a block diagram of multiport, multipurpose network integrated circuit (chip) 200. No processor or CPU is shown.

Also, Beaudoin very specifically states that it is an object of the invention not to utilize a processor or CPU when implementing the functionality of multiport, multipurpose network integrated circuit (chip) 200. Specifically, Beaudoin states the following: "It is an object of the present invention to provide apparatus and methods for hardware control of network switching functions rather than CPU based control." See column 2, lines 55 through 57.

Claim 1 does not merely state that the chip includes an embedded processor. Claim 1 also particularly points out various features of the embedded processor. Claim 1 indicates the embedded processor is between the host interface and the media access controller. The embedded processor is programmable to function as a manageability web server, communicate with the host interface and obtain manageability information about the network device. The embedded processor further is programmable to send the manageability information to the media access controller for transmission over the computer network. None of this functionality is disclosed or suggested by Beaudoin.

Applicant notes that Beaudoin does not specifically indicate that circuit 200 includes an embedded processor. Examiner is apparently only inferring the existence of an embedded processor within Beaudoin. However, nothing in Beaudoin could be take to infer, for example, that any embedded processor within circuit 200 would be programmable to function as a manageability web server, as set out in claim 1 of the present application. Beaudoin does not even mention the web or the internet.

Host Interface

The chip set out in claim 1 also includes a host interface connectable to the host processor.

Examiner has based his argument for the existence of an embedded processor within multiport, multipurpose network integrated circuit (chip) 200 on there being no host processor. Specifically, Examiner has argued as follows:

> If there is not need for external processor in Beaudoin, then an absence of an external processor indicates that Beaudoin discloses a processor on single chip 200...

Examiner also asserts (without support) that the network device includes a host processor, and assumes that multiport, multipurpose network integrated circuit (chip) 200 includes a host interface connectable to the host processor. Where in Figure 1 is the host processor or the host interface disclosed? If these are disclosed in Figure 1, what does this do to Examiner's argument for the existence of an embedded processor?

**Discussion of Independent Claim 13**

Independent claim 13 sets out a network device. The network device includes a chip. The chip includes a media access controller, an interchip communications interface and an embedded processor.

Non-volatile memory is programmed with a plurality of executable instructions. The instructions, when executed, instructs the embedded processor to function as a manageability web server, communicate with the interchip communications means to obtain manageability information about

the compliant device, and send the manageability information to the media access controller for transmission over the computer network. This functionality is not disclosed or suggested by the cited art.

The Examiner has asserted that Circuit 200 of Beaudoin includes an embedded processor. As discussed above, Examiner appears to be making this assertion based on the statement by Beaudoin at column 15, lines 5 through 7: "More particularly, this consolidation results in the elimination of the need for an external CPU to control, or coordinate control, of all these functions."

However, this statement in Beaudoin does not specifically state that Circuit 200 includes an embedded processor, but only indicates that there is no need for an external CPU to control or coordinate control of functions performed by circuit 200.

As discussed above, Figure 1 includes a block diagram of multiport, multipurpose network integrated circuit (chip) 200. No processor or CPU is shown.

Also, Beaudoin very specifically states that it is an object of the invention not to utilize a processor or CPU when implementing the functionality of multiport, multipurpose network integrated circuit (chip) 200. Specifically, Beaudoin states the following: "It is an object of the present invention to provide apparatus and methods for hardware control of network switching functions rather than CPU based control." See column 2, lines 55 through 57.

Applicant notes that claim 13 does not merely state that the chip includes an embedded processor. Claim 13 also particularly points out various features of the embedded processor. Claim 13 indicates the embedded processor is instructed to function as a manageability web server, communicate with the interchip communications means to obtain manageability information about the compliant device, and send the manageability information to the media access controller for transmission over the computer network. None of this functionality is disclosed or suggested by Beaudoin.

Further, nothing in Beaudoin could be take to infer, for example, that any embedded processor within circuit 200 would be programmable to function as a manageability web server, as set out in claim 13 of the present application. Beaudoin does not even mention the web or the internet.

**Discussion of Independent Claim 23**

Independent claim 23 sets out a system. The system includes a network device. The network device includes a chip. The chip includes a media access controller and an embedded processor programmed to function as an HTTP manageability web server. This functionality is not disclosed or suggested by the cited art.

The Examiner has asserted that Circuit 200 of Beaudoin includes an embedded processor. As discussed above, Examiner appears to be making this assertion based on the statement by Beaudoin at column 15, lines 5 through 7: "More particularly, this consolidation results in the elimination of

the need for an external CPU to control, or coordinate control, of all these functions."

However, this statement in Beaudoin does not specifically state that Circuit 200 includes an embedded processor, but only indicates that there is no need for an external CPU to control or coordinate control of functions performed by circuit 200.

As discussed above, Figure 1 includes a block diagram of multiport, multipurpose network integrated circuit (chip) 200. No processor or CPU is shown.

Also, Beaudoin very specifically states that it is an object of the invention not to utilize a processor or CPU when implementing the functionality of multiport, multipurpose network integrated circuit (chip) 200. Specifically, Beaudoin states the following: "It is an object of the present invention to provide apparatus and methods for hardware control of network switching functions rather than CPU based control." See column 2, lines 55 through 57.

Claim 23 also particularly points out various features of the embedded processor. Claim 23 indicates the embedded processor is programmed to function as an HTTP manageability web server. This functionality is disclosed or suggested by Beaudoin. Nothing in Beaudoin could be taken to infer that any embedded processor within circuit 200 is programmed to function as an HTTP manageability web server, as set out in claim 23 of the present application. Beaudoin does not even mention the web or the internet.

## Conclusion

Applicant believes that the present Application is in condition for allowance and favorable action is respectfully requested.

Respectfully submitted,
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